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Assistant Commissioner for Patents
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Washington, D.C. 20231

Sir:

As authorized by the inventor(s), transmitted herewith for filing is a patent application applied for on behalf of the inventor(s) according to the provisions of 37 CFR 1.41(c).

Inventor(s): SONG, In Duk
YOON, Won Gyun; KWON, Keuk Sang

For: THIN FILM TRANSISTOR SUBSTRATE OF LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURE

Enclosed are:

X A specification consisting of 18 pages

X 05 sheet(s) of Formal drawings

X Certified copy of Priority Document(s)

X Executed Declaration in accordance with 37 CFR 1.64 will follow

___ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27

___ Preliminary Amendment

X Information Sheet

X Information Disclosure Statement, PTO-1449 with reference(s)

___ Other ____

The filing fee has been calculated as shown below:

FOR	NO. FILED	NO. EXTRA	LARGE ENTITY RATE	LARGE ENTITY FEE		SMALL ENTITY RATE	SMALL ENTITY FEE
BASIC FEE	*********** *********** ***********	********** ********** **********	***** ***** *****	$690.00	or	**** **** ****	$345.00
TOTAL CLAIMS	31 - 20 =	11	x18 =$	198.00	or	x 9 = $	0.00
INDEPENDENT	3 - 3 =	0	x78 =$	0.00	or	x 39 = $	0.00
MULTIPLE DEPENDENT CLAIM PRESENTED	no		+260 = $	0.00	or	+130 = $	0.00
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X The application transmitted herewith is filed in accordance with 37 CFR 1.41(c). The undersigned has been authorized by the inventor(s) to file the present application. The original duly executed patent application together with the surcharge will be forwarded in due course.

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Respectfully submitted,

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THIN FILM TRANSISTOR SUBSTRATE OF LIQUID CRYSTAL DISPLAY AND METHOD OF MANUFACTURE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a liquid crystal display, and more particularly to a thin film transistor substrate, which has increased aperture ratio, prevents shorts between pixel electrodes and/or reduces the number of holes for contacting the pixel electrodes, and a method of manufacturing the thin film transistor substrate.

Description of the Related Art

Generally, a liquid crystal display (LCD) displays a picture by controlling light transmissivity using an electric field. To this end, the LCD includes a liquid crystal panel having liquid crystal cells arranged in a matrix, and a driving circuit for driving the liquid crystal panel. The liquid crystal panel is provided with pixel electrodes for applying an electric field to each liquid crystal cell with respect to a reference electrode, that is, a common electrode. Typically, the pixel electrodes are provided on a lower substrate for each liquid crystal cell, whereas the common electrode is integrally formed on the entire surface of an upper, opposing substrate. Each of the pixel electrodes is connected to a thin film transistor (TFT) used as a switching device. The pixel electrode drives the liquid crystal cell in accordance with a data signal applied via the TFT.

Fig. 1 shows an electrode arrangement of a thin film transistor substrate of a conventional liquid crystal display. In Fig. 1, the LCD includes thin film transistors 8 positioned at the intersections between data lines 4 and gate lines 2,

and pixel electrodes 6 connected to drain electrodes 14 of the thin film transistors 8. Each of the thin film transistors 8 includes a gate electrode 10 protruding from the gate line 2, a source electrode 12 protruding from the data line 4, and the drain electrode 14 connected to the pixel electrode 6 via a first contact hole 20. Further, each thin film transistor 8 includes a gate-insulating film (not shown) insulating the gate electrode 10 from a semiconductor layer (not shown), which defines a conductive channel between the source electrode 12 and the drain electrode 14 when a large enough gate voltage is applied to the gate electrode 10. The thin film transistor 8 responds to a gate signal from the gate line 2 to selectively apply a data signal from the data line 2 to the pixel electrode 6.

The pixel electrode 6 is located at a cell area defined by the data line 4 and the gate line 2 and is made from an ITO (indium tin oxide) with a high light transmissivity. The pixel electrode 6 is formed on a protective film (not shown) coated on the entire surface of the thin film transistor 8, and is electrically connected, via the first contact hole 20 formed in the protective film, to the drain electrode 14. The pixel electrode 6 generates a potential difference with respect to a common transparent electrode (not shown) provided at an upper substrate, opposing the thin film transistor substrate, in response to a data signal applied via the thin film transistor 8. By this potential difference, liquid crystal positioned between the thin film transistor substrate and the upper substrate is rotated to allow light, from a light source, to pass therethrough.

As further shown in Fig. 1, storage capacitor 18 and the prior or pre-stage gate line 2 are overlapped by a portion of the pixel electrode 6. The storage capacitor 18 prevents a voltage variation in the pixel electrode 6 by charging to a voltage when a gate high voltage is applied to the pre-stage gate line 2 and discharging the charge voltage when a data

signal is applied to the pixel electrode 6. The storage capacitor 18 must have a large capacitance value so as to maintain a stable pixel voltage. To this end, the storage capacitor 18 is formed by the pre-stage gate line 2, an overlapping storage electrode 16, and the gate insulating film (not shown) disposed therebetween. The storage electrode 16 is electrically connected, via a second contact hole 22 formed in the protective film (not shown), to the pixel electrode 6. The storage electrode 16 is provided on the gate insulating film at the time of forming the data line 4 and the source and drain electrodes 12 and 14.

As described above, in the conventional thin film transistor substrate, the overlapping portion of the pixel electrode 6 and the pre-stage gate line 2 must be as large as possible so as to provide a storage capacitor with a large capacitance value. As a result, the distance between the pixels 6 adjacent to each other at the upper and lower portions thereof is reduced, and a short may be generated between them.

Also, inorganic film with a large dielectric constant, such as SiN_x, and SiO_x, is usually used for the protective film of the thin film transistor substrate. This inorganic protective film typically maintains a constant horizontal interval (e.g., 3 to 5 μm) between the pixel electrode 6 and the data line 4 to minimize a coupling effect caused by a parasitic capacitor Cds.

However, during processing, particularly the several light-exposing steps, miss alignment errors can occur between electrodes formed from different layers. As a result, a constant interval may not be maintained between the data line 4 and the pixel electrode 6, and a capacitance of the parasitic capacitor Cds between the data line 4 and the pixel electrode 6 becomes non-uniform. A data signal, applied to the data line 4 and then to the pixel electrode 6 is deteriorated due to the coupling effect caused by this non-uniform

parasitic capacitor Cds, and picture quality thus deteriorates.

Furthermore, in the conventional LCD, an aperture ratio is reduced by as much as the drain electrode 14 of the thin film transistor 8 overlaps the pixel electrode 6 for formation of the contact hole 20.

SUMMARY OF THE INVENTION

The thin film transistor substrate according to the present invention includes a plurality of gate lines formed on a substrate and a plurality of data lines insulated from and intersecting the gate lines. The data lines and intersecting gate lines define a plurality of cells. At least one cell includes a pixel electrode, a thin film transistor connected to one of the data lines and one of the gate lines defining the cell, a storage capacitor, and a metallic pattern forming a drain electrode of the thin film transistor and a storage electrode of the storage capacitor.

In one embodiment, the metallic pattern is electrically connected to the pixel electrode at the storage electrode part. Because the storage electrode part is electrically connected to the drain electrode part, no separate connection between the drain electrode and the pixel electrode is required. As a result, the size of the drain electrode is reduced, the effective size of the pixel electrode is increased, and the aperature ratio of the thin film transistor substrate is increased.

In another embodiment, the metallic pattern is electrically connected to the pixel electrode at the drain electrode part. Because the drain electrode part is electrically connected to the storage electrode part, no separate connection between the storage electrode and the pixel electrode is required. As a result, the pixel electrode does not need to overlap the pre-stage gate line, and shorts caused by adjacent pixel electrodes being too closely spaced can be eliminated.

In yet another embodiment, the metallic pattern is electrically connected to the pixel electrode at both the drain and storage electrode parts. Preferably, in this embodiment, the metallic pattern has an annular shape approximating the periphery of the pixel electrode, and therefore, prevents light from leaking from the cell.

Preferably, in each of the embodiments, the data lines and metallic pattern are formed simultaneously from the same conductive material such that a constant predetermined minimum spacing is achieved between the metallic pattern and an adjacent data line. Consequently, a uniform parasitic capacitor, formed by the metallic pattern and the adjacent data line, is obtained, and the deterioration of the data signal is prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

The achieved advantages of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in which:

Fig. 1 illustrates an electrode arrangement of a thin film transistor substrate in a conventional liquid crystal display;

Fig. 2 illustrates an electrode arrangement of a thin film transistor substrate according to an embodiment of the present invention;

Fig. 3 illustrates an electrode arrangement of a thin film transistor substrate according to a further embodiment of the present invention;

Fig. 4 illustrates an electrode arrangement of a thin film transistor substrate according to another embodiment of the present invention; and

Fig. 5 illustrates an electrode arrangement of a thin film transistor substrate according to still another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to Fig. 2, there is shown an electrode arrangement of a thin film transistor substrate in a liquid crystal display according to a first embodiment of the present invention. For those elements not specifically mentioned or discussed in detail, it is to be understood that those elements are the same as in the conventional art described with respect to Fig. 1.

As shown, the liquid crystal display includes thin film transistors 30 positioned at intersections between data lines 26 and gate lines 24, and pixel electrodes 28 connected, via drain electrode patterns 36, to the thin film transistors 30. Each of the thin film transistors 30 includes a gate electrode 32 protruding from the gate line 24, a source electrode 34 protruded from the data line 26 and the drain electrode pattern 36. A gate insulating film (not shown) insulates the gate electrode 32 from the source and drain electrodes 34 and 36 and a semiconductor layer (not shown), which forms a conductive channel between the source electrode 34 and the drain electrode pattern 36 when a gate voltage is applied to the gate electrode 32.

The drain electrode pattern 36 is formed such that it overlaps a portion of the periphery of the pixel electrode 28. The drain electrode pattern 36 includes a drain electrode part 36A and a storage electrode part 36B. The drain electrode part 36A forms the drain electrode of the thin film transistor 30, and the storage electrode part 36B forms a part of a storage capacitor 38. A portion of the storage electrode part 36B overlaps part of the pre-stage gate line 24, is partially overlapped by the pixel electrode 28, and is connected, via a contact hole 40 formed in a protective film (not shown) between the storage electrode part 36B and the pixel electrode 28, to the pixel electrode 28. Accordingly, the contact hole for connecting the pixel electrode 28 to the drain electrode

(i.e., the drain electrode part 36A) can be eliminated. This allows for reduction in the size of the drain electrode, and eliminates the need for the pixel electrode 28 to overlap the drain electrode part 36A. As a result, the size of the pixel electrode 28 is increased, and the aperture ratio of liquid crystal cell is increased.

The storage electrode part 36B of the drain electrode pattern 36 forms the storage capacitor 38 along with the overlapped pre-stage gate line 24 and the gate insulating film formed therebetween. Such a drain electrode pattern 36 has a relatively small width at a portion close to the data line 26 such that it is not shorted to the data line 26. Because the drain electrode pattern 36 and the data line 26 are formed from the same conductive layer during processing, (1) a constant separation interval is formed between the drain electrode pattern 36 and the data line 26, and (2) a parasitic capacitor Cds between the data line 26 and the drain electrode pattern 36 is consistently or uniformly maintained. As a result, deterioration of the data signal caused by the non-uniformity of the parasitic capacitor Cds is prevented. Also, the storage electrode part 36B of the drain electrode pattern 36 has a large width so as to provide the storage capacitor 38 with a larger capacitance value.

The thin film transistor 30 responds to the gate signal from the gate line 24 to selectively apply the data signal from the data line 26 to the pixel electrode 28. The pixel electrode 28, located at a cell area defined by the data line 26 and the gate line 24, is made from an ITO (indium tin oxide) material with a high light transmissivity. The pixel electrode 28 is formed on a protective film (not shown) coated over an entire surface of the thin film transistor substrate. The pixel electrode 28 generates a potential difference with respect to a common transparent electrode (not shown) provided at the upper, opposing substrate in response to a data signal applied via the thin film transistor 30. By this potential

difference, liquid crystal positioned between the thin film transistor substrate and the upper substrate is rotated by its dielectric anisotropy to allow light, to pass therethrough. The storage capacitor 38 prevents a voltage variation in the pixel electrode 28 by charging to a voltage when a gate high voltage is applied to the pre-stage gate line 24 and discharging the charge voltage when a data signal is applied to the pixel electrode 28.

A method of fabricating the thin film transistor substrate having the configuration as mentioned above will be described. After a gate metal layer is deposited on a transparent substrate and patterned to form the gate line 24 and the gate electrode 32, a gate insulating film is coated over the substrate. After an amorphous silicon layer is formed on the gate insulating film and patterned to form a semiconductor layer of the thin film transistor 30, a source/drain metal layer is deposited and then patterned to form the data line 26, the source electrode 34 and the drain electrode pattern 36 at the same time. Subsequently, a protective film is coated over the substrate and patterned to form the contact holes 40. Finally, a transparent electrode material is coated on the protective film and then patterned to form the pixel electrode 28.

Referring to Fig. 3, there is shown an electrode arrangement of a thin film transistor substrate in a liquid crystal display according to a second embodiment of the present invention. When compared with the thin film transistor shown in Fig. 2, the thin film transistor substrate of Fig. 3 has the same constructional elements except that the drain electrode pattern 42 is electrically connected via a contact hole 44 to the pixel electrode 28 at a drain electrode part 42A. Accordingly, the contact hole for connecting the pixel electrode 28 to storage electrode part 42B is eliminated to reduce an amount of overlap between the storage electrode part 42B and the pixel electrode 28.

In this embodiment, because the amount or width of the pixel electrode 28 overlapping the storage electrode part 42B of the drain electrode pattern 42 is reduced from 15 to 20μm in the prior art to 2 to 4μm, a potential short between the upper and lower pixel electrodes 28 can be prevented. Also, the drain electrode pattern 42 and the data line 26 are formed from the same layer with a uniform interval therebetween to uniformly maintain a parasitic capacitor Cds between the drain electrode 26 and the drain electrode pattern 42. Therefore, a deterioration of the data signal caused by a non-uniformity of the parasitic capacitor Cds is prevented.

The thin film transistor substrate of Fig. 3 is formed by the same method as described with respect to Fig. 2, except that the protective film is patterned to form the contact holes 44 and the pixel electrodes 28 are formed to have the shape shown in Fig. 3.

Referring to Fig. 4, there is shown an electrode arrangement of a thin film transistor substrate in a liquid crystal display according to a third embodiment of the present invention. When compared with the thin film transistor shown in Fig. 3, the thin film transistor substrate of Fig. 4 has the same constructional elements except that a drain electrode pattern 46 is formed to have an annular shape along the periphery of the pixel electrode 28. In this case, the drain electrode pattern 46 is formed in an annular shape and overlaps with the bottom periphery of the pixel electrode 28; unlike the U-shaped drain electrode patterns 36 and 42 in Fig. 2 and Fig. 3, respectively.

The drain electrode pattern 46 prevents light from leaking between the pixel electrode 28 and the gate line 24. The drain electrode pattern 46 is connected, via a contact hole 48 formed in a protective film on the drain electrode part 46A, to the pixel electrode 28. Accordingly, the contact hole for connecting the storage electrode part 46B to the

pixel electrode 28 can be eliminated to reduce a width or amount by which the pixel electrode 28 overlaps with the storage electrode part 42B. This then prevents a short between the upper and lower pixel electrodes 28.

Alternatively, the drain electrode pattern 46 may be connected to the pixel electrode 28 by forming a contact hole (not shown) in the protective film on the storage electrode part 46B. In this alternative, the contact hole for connecting the drain electrode part 46A of the drain electrode pattern 46 to the pixel electrode 28 can be eliminated to reduce to the size of the drain electrode part 46A, to increase an effective size of the pixel electrode 28 while reducing an area of the pixel electrode 28 overlapping the drain electrode part 46A, and to thus increase an aperture ratio of liquid crystal cell. The drain electrode pattern 46 is also uniformly spaced from the data line 26 to uniformly maintain a parasitic capacitor Cds between the drain electrode 26 and the drain electrode pattern 46. Therefore, a deterioration of the data signal caused by a non-uniformity of the parasitic capacitor Cds is prevented.

The thin film transistor substrate of Fig. 4 is formed by the same method as described with respect to Fig. 2, except for patterning certain layers to achieve the above noted structural differences.

Referring to Fig. 5, there is shown an electrode arrangement of a thin film transistor substrate in a liquid crystal display according to a fourth embodiment of the present invention. When compared with the thin film transistor shown in Fig. 3, the thin film transistor substrate of Fig. 5 has the same constructional elements except that a drain electrode pattern 50 is electrically connected, via contact holes 52 and 54, to the pixel electrode 28 at a drain electrode part 50A and a storage electrode part 50B, respectively. The drain electrode pattern 50 is electrically connected, via the contact hole 52 formed in a protective film

on the drain electrode part 50A, to the pixel electrode 28 and, at the same time, is electrically connected, via the contact hole 54 formed in a protective film on the storage electrode part 50B, to the pixel electrode 28. Also, the drain electrode pattern 50 and the data line 26 are formed from the same conductive layer during processing and at a constant separation interval to uniformly maintain a parasitic capacitor Cds between the drain electrode 26 and the drain electrode pattern 50. Therefore, a deterioration of the data signal caused by a non-uniformity of the parasitic capacitor Cds is prevented.

The thin film transistor substrate of Fig. 5 is formed by the same method as described with respect to Fig. 2, except for patterning certain layers to achieve the above noted structural differences.

As described above, according to embodiments of the present invention, the drain electrodes are connected to the storage electrodes in a manner to reduce the number of contact holes, increase an aperture ratio, and prevent shorts between pixel electrodes. Also, a space between the data line and the drain electrode pattern connected to the pixel electrode becomes consistent to maintain a uniform parasitic capacitor Cds and prevent deterioration of the data signal caused by a non-uniformity of the parasitic capacitor Cds.

Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather, various changes or modifications thereof are possible without departing from the spirit of the invention.

What is claimed is:

1. A thin film transistor substrate, comprising:

a plurality of gate lines formed on a substrate;

a plurality of data lines insulated from and intersecting said gate lines, said data lines and intersecting gate lines defining a plurality of cells, at least one cell including,

a pixel electrode,

a thin film transistor connected to one of the data lines and one of the gate lines defining the cell,

a storage capacitor, and

a metallic pattern forming a drain electrode of the thin film transistor and a storage electrode of the storage capacitor, and being electrically connected to the pixel electrode.

2. The substrate of claim 1, wherein the metallic pattern is spaced a predetermined distance from the data line connected to the thin film transistor.

3. The substrate of claim 2, further comprising:

a protective layer disposed between the pixel electrode and the metallic pattern, the metallic pattern being overlapped with a portion of a periphery of the pixel electrode.

4. The substrate of claim 1, further comprising:

a protective layer disposed between the pixel electrode and the metallic pattern, the metallic pattern being overlapped with a portion of a periphery of the pixel electrode.

5. The substrate of claim 4, wherein

the metallic pattern has an annular shape, and

an entire periphery of the pixel electrode overlaps the

metallic pattern.

6. The substrate of claim 5, wherein the metallic pattern is spaced a predetermined distance from the data line connected to the thin film transistor.

7. The substrate of claim 1, further comprising:

a protective layer disposed between the pixel electrode and the metallic pattern, the pixel electrode being connected to a source electrode part of the metallic pattern via a first contact hole in the protective layer.

8. The substrate of claim 7, wherein the protective layer does not include a contact hole over a drain electrode part of the metallic pattern.

9. The substrate of claim 8, wherein the drain electrode part has a smaller area than if the drain electrode part was electrically connected to the pixel electrode via a contact hole in the protective layer over the drain electrode part.

10. The substrate of claim 8, wherein the pixel electrode has a larger aspect ratio than if the drain electrode part was electrically connected to the pixel electrode via a contact hole in the protective layer over the drain electrode part.

11. The substrate of claim 8, wherein

the metallic pattern is spaced a predetermined distance from the data line connected to the thin film transistor; and

a portion of a periphery of the pixel electrode overlaps the metallic pattern.

12. The substrate of claim 8, wherein

the metallic pattern has an annular shape and is spaced a predetermined distance from the data line connected to the

thin film transistor; and

an entire periphery of the pixel electrode overlaps the metallic pattern.

13. The substrate of claim 7, wherein

the pixel electrode is connected to a drain electrode part of the metallic pattern via a second contact hole in the protective layer.

14. The substrate of claim 13, wherein

the metallic pattern is spaced a predetermined distance from the data line connected to the thin film transistor; and

a portion of a periphery of the pixel electrode overlaps the metallic pattern.

15. The substrate of claim 13, wherein

the metallic pattern has an annular shape and is spaced a predetermined distance from the data line connected to the thin film transistor; and

an entire periphery of the pixel electrode overlaps the metallic pattern.

16. The substrate of claim 1, further comprising:

a protective layer disposed between the pixel electrode and the metallic pattern, and wherein

the pixel electrode is connected to a drain electrode part of the metallic pattern via a contact hole in the protective layer.

17. The substrate of claim 16, wherein the protective layer does not include a contact hole over a source electrode part of the metallic pattern.

18. The substrate of claim 17, wherein the pixel electrode overlaps a gate line, defining the cell but not

connected to the thin film transistor, less than if the protective layer included a contact hole over a storage electrode part of the metallic pattern.

19. The substrate of claim 17, wherein

the metallic pattern is spaced a predetermined distance from the data line connected to the thin film transistor; and

a portion of a periphery of the pixel electrode overlaps the metallic pattern.

20. The substrate of claim 16, wherein

the metallic pattern has an annular shape and is spaced a predetermined distance from the data line connected to the thin film transistor; and

an entire periphery of the pixel electrode overlaps the metallic pattern.

21. A thin film transistor substrate, comprising:

a plurality of gate lines formed on a substrate;

a plurality of data lines insulated from and intersecting said gate lines, said data lines and intersecting gate lines defining a plurality of cells, at least one cell including,

a pixel electrode,

a thin film transistor selectively electrically connecting one of the data lines to the pixel electrode, and including a source electrode connected to the one of the data lines, a gate electrode connected to one of the gate lines, and a drain electrode, and

a storage capacitor having a storage electrode electrically connected to the drain electrode and the pixel electrode.

22. The substrate of claim 21, further comprising:

a metallic pattern connecting the storage electrode and the drain electrode.

23. A method of manufacturing a thin film transistor substrate, comprising:

forming a plurality gate lines with gate electrodes extending therefrom on a transparent substrate;

forming a gate insulating layer over the substrate;

forming a plurality of data lines intersecting with the gate lines over the substrate, the data lines including source electrodes extending therefrom;

forming a metallic pattern having a drain electrode part and a source electrode part, the source electrode part formed overlapping with one of the gate lines;

forming a semiconductor layer over at least a portion of one of the gate electrodes, at least a portion of one of the source electrodes, and at least a portion of the drain electrode part;

forming a protective film over the substrate, the protective film including a contact hole exposing a portion of the metallic pattern; and

forming a pixel electrode over the protective film and in electrical contact with the metallic pattern via the contact hole.

24. The method of claim 23, wherein the forming a plurality of data lines step and the forming a metallic pattern step are performed simultaneously by forming a conductive layer over the substrate and patterning the conductive layer to form the data lines and the metallic pattern such that the metallic pattern is spaced a predetermined distance from one of the data lines.

25. The method of claim 23, wherein the forming a pixel electrode step forms the pixel electrode such that a portion of a periphery of the pixel electrode overlaps the metallic pattern.

26. The method of claim 23, wherein the forming a pixel electrode step forms the pixel electrode such that an entire periphery of the pixel electrode overlaps the metallic pattern.

27. The method of claim 23, wherein the forming a protective layer step forms the protective layer with a first contact hole exposing the source electrode part of the metallic pattern.

28. The method of claim 27, wherein the forming a protective layer step does not form the protective layer with a contact hole exposing the drain electrode part of the metallic pattern.

29. The method of claim 27, wherein the forming a protective layer step forms the protective layer with a second contact hole exposing the drain electrode part of the metallic pattern.

30. The method of claim 23, wherein the forming a protective layer step forms the protective layer with a contact hole exposing the drain electrode part of the metallic pattern.

31. The method of claim 30, wherein the forming a protective layer step does not form the protective layer with a contact hole exposing the source electrode part of the metallic pattern.

Abstract

The thin film transistor substrate increases an aperture ratio as well as prevents shorts between pixel electrodes by connecting drain electrodes of thin film transistors to storage electrodes to reduce the number of holes contacting the pixel electrodes. In the method of forming the thin film transistor substrate, drain electrode patterns are formed such that drain electrodes included in thin film transistors are electrically connected to storage electrodes included in storage capacitors. Accordingly, the number of holes contacting the pixel electrodes can be reduced so that an aperture ratio can be increased, or shorts between pixel electrodes can be prevented. Also, the drain electrode patterns are formed from the same conductive layer as the data lines supplying data signals to the thin film transistors, and a constant spacing between the two can be obtained to maintain a uniform parasitic capacitance therebetween and prevent deterioration of the data signal.

FIG. 1
CONVENTIONAL ART

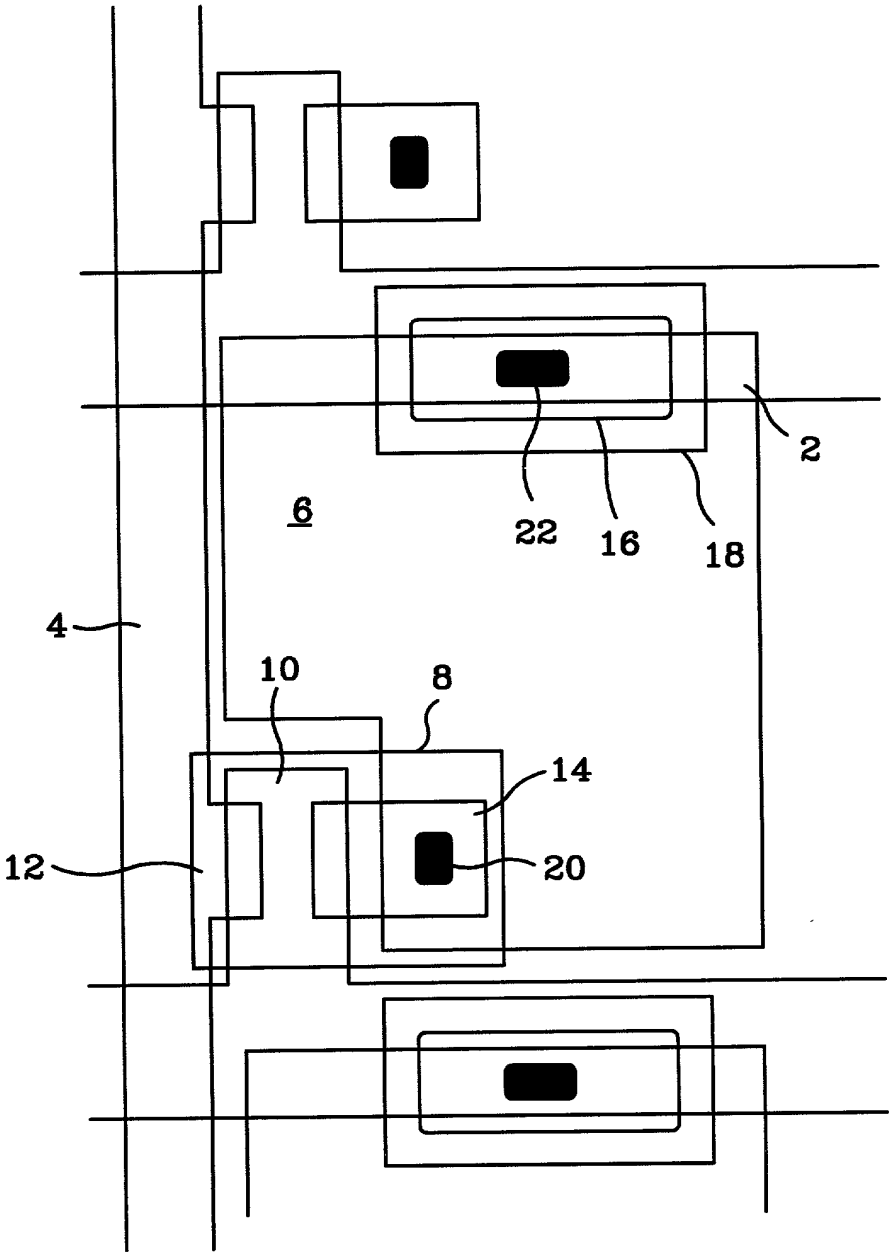

FIG.2

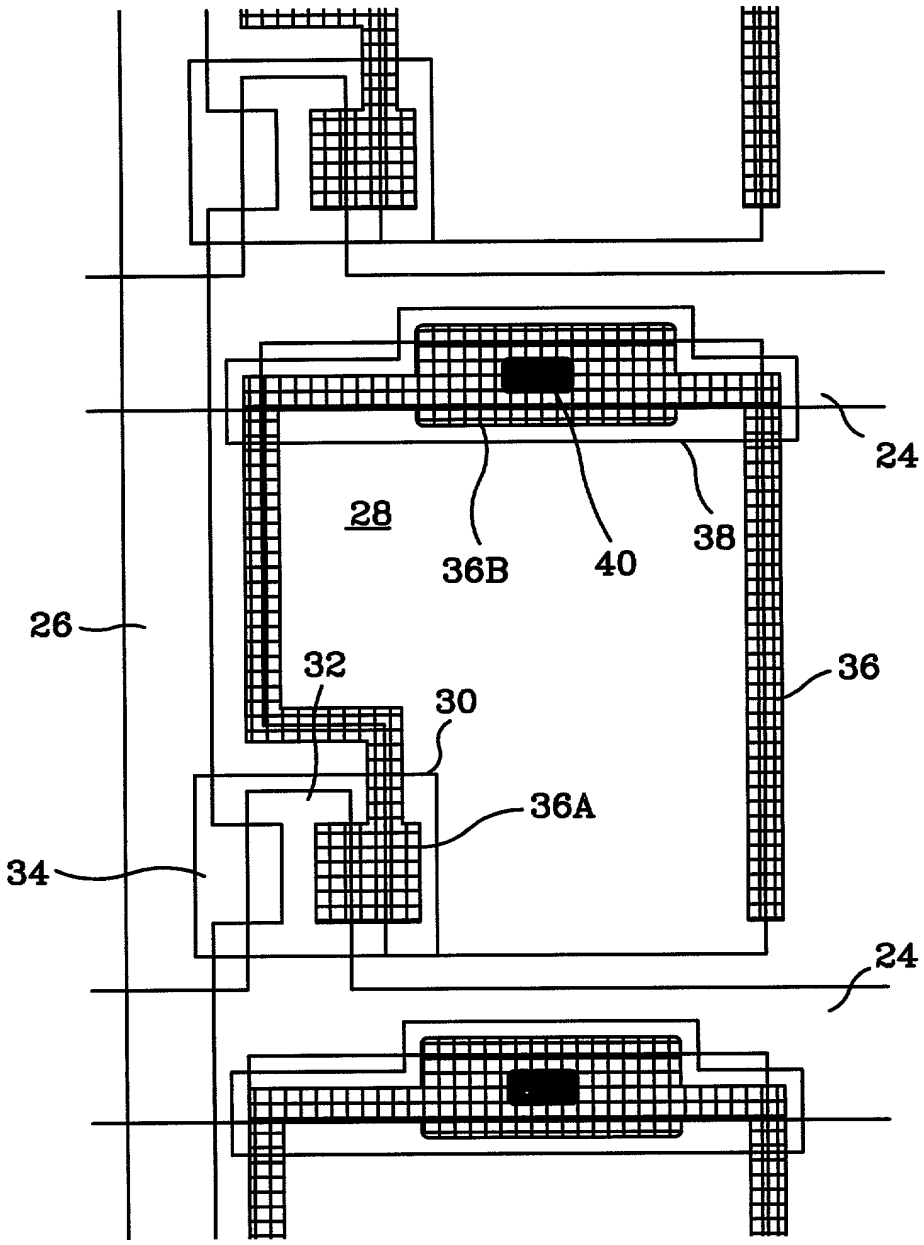

FIG.3

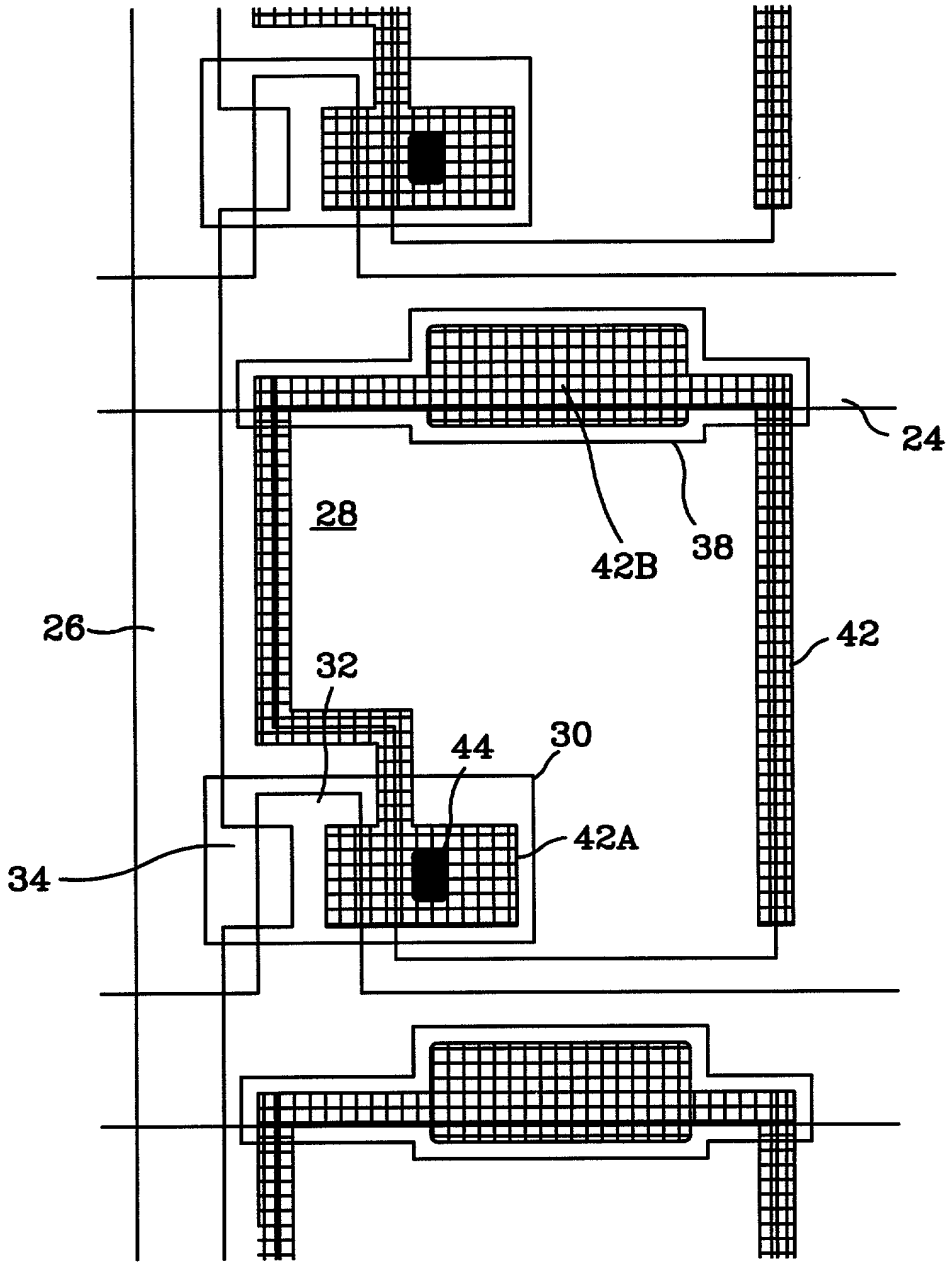

FIG. 4

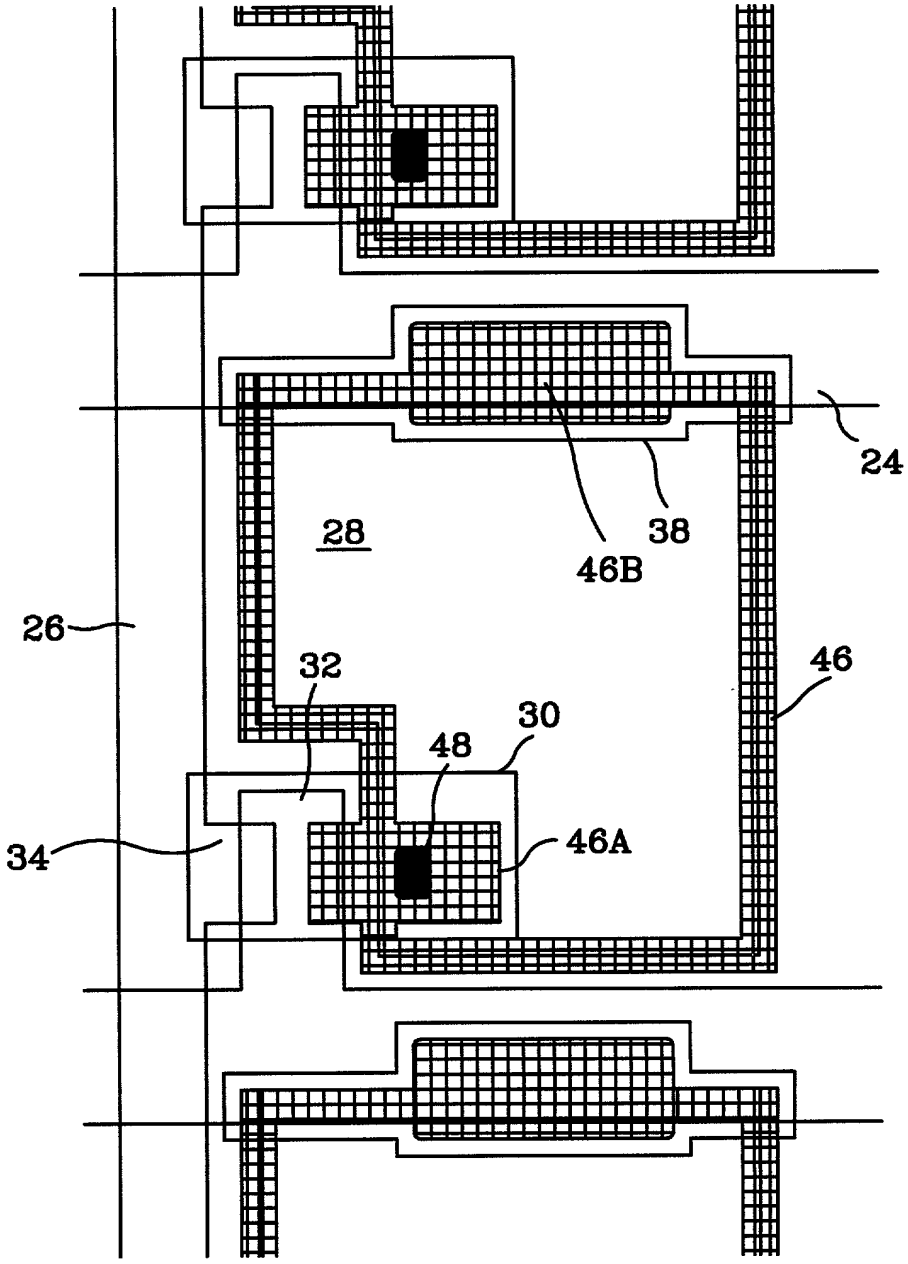

FIG.5